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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/716,008

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EXAMINER

SENGI, BEHROOZ M

ART UNIT

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12/01/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/716,008	Applicant(s) RAMAKRISHNAN ET AL.	
	Examiner BEHROOZ SENFI	Art Unit 2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11/17/2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3,5,7 and 9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,5,7 and 9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/13/2008 has been entered.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1, 3 and 9 are rejected under 35 U.S.C. 101 because; the claimed invention is directed to non-statutory subject matter.

Regarding claims 1 and 3, it is noted that the invention as claimed is directed to "a method for storing macro-blocks in a memory, thus comprises decoding process". Such invention is non- statutory; because the process of storing macro-blocks including decoding a macro-block as claimed fails to positively tie to another statutory class by the claim. Therefore; such invention is not a patent eligible process under Memorandum, dated May 15, 2008, subject of clarification of "processes" under 35 USC 101.

Claim 9 is rejected under 35 U.S.C. 101 by virtue of their dependency to independent claim 18.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 9 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is noted that in the newly added limitations, wherein “one portion of a single data word is part of the second portion and another portion of the single data word is part of the third portion form” was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant fails to explicitly explain the above subject matter “one portion of a single data word is part of the second portion and another portion of the single data word is part of the third portion form” in a clear and concise language in the specification of the present application. Therefore, the claims are rejected as best understood by the examiner.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1, 3, 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (US 7,079,583) in view of Uchida (US 5,461,486).

Regarding claim 1, Yoshioka '583 discloses, a method for storing macro-blocks in a memory (i.e., fig. 3, memory 3 is used for storing macro-blocks), the method comprising;

decoding a macro-block, thereby resulting in a decoded macro-block, the decoded macro-block comprising pixels (i.e., fig. 3, decoder 1002 including routine processing 1004 used for decoding a macro-block, see col. 11, lines 21 – 44 and col. 16, lines 12 – 13); and executing an instruction, wherein the instruction causes writing the decoded macro-block to the memory (i.e., fig. 3, illustrates decoder unit 1002 including, routine processing unit 1004 execute the received instruction from processing unit 1003 to perform decode processing on macro-block and stores, e.g., writes the decoded block/macro-block to the memory unit 3, see col. 11, lines 39 – 50).

Although, Yoshioka '583 show writing decoded macro-block composed of writing decoded luminance matrix blocks (Y) and decoded chrominance matrix blocks (Cb) and (Cr) to the memory.

Yoshioka '583 is silent in regards to explicit of arrangement for writing the decoded macro-block in the, “first portion of the memory; second portion of the memory; third portion of the memory; and the first portion, second portion, and third portion being contiguous”.

Uchida '486 teaches the above-mentioned claimed limitations are well known in the art. In particular, Uchida '486 teaches the arrangement of writing a matrix of

Art Unit: 2621

luminance to a first portion of the memory (i.e., as shown in figs. 3 and 11, the DCT blocks of luminance matrix Y are stored in the respective memory areas assigned to, e.g., first portion of memory, see col. 7, lines 27 – 41 and lines 55 – 60); writing a first matrix of chrominance to second portion of the memory (i.e., as shown in figs. 3 and 11, the DCT blocks of the color difference R-Y, e.g., first matrix of chrominance (Cr) stored in the respective memory area assigned thereto, e.g., second portion of memory, see col. 7, lines 26 – 41 and lines 55 – 60); writing a matrix of second chrominance to a third portion of the memory (i.e., as shown in fig. 11, the DCT blocks of second chrominance matrix B-Y (Cb) written in the respective memory area assigned thereto, e.g., third portion of the memory, see col. 7, lines 27 – 41 and lines 55 – 60); and the first portion, second portion, and third portion being contiguous (i.e., as shown in fig. 11, the first portion (Y), second portion (R-Y) and third portion (B-Y) of the memory are arranged in continuous/contiguous form).

In view of the above, having the digital signal processing of Yoshioka showing writing decoded macro-block composed of luminance blocks (Y) and chrominance blocks (Cb) and (Cr) to the memory, and given the well-established teaching of Uchida where the luminance matrix is written in a first portion of the memory; and first chrominance matrix to second portion of the memory and a second chrominance matrix to a third portion of the memory, where the first portion, second portion, and third portion being contiguous, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the digital signal processing of Yoshioka as taught by Uchida, since Uchida suggest in col. 2, lines 57 – 58 that such a

Art Unit: 2621

modification would improved image quality in the high speed reproduction of the recorded digital video signal.

Regarding claim 3, Yoshioka '583 teaches, a method for storing macro-blocks In a memory (i.e., fig. 3, memory 3 is used for storing macro-blocks), the method comprising;

decoding macro-blocks, thereby resulting in decoded macro-blocks, the decoded macro-blocks comprising pixels (i.e., fig. 3, decoder 1002 including routine processing 1004 used for decoding a macro-blocks, see col. 11, lines 40 – 43 and col. 16, lines 12 – 13); and executing an instruction, wherein the instruction causes writing the macro-blocks to the memory (i.e., fig. 3, describes routine processing unit 1004 execute the received instruction from processing unit 1003 to perform decode processing on macro-blocks and stores/writes the decoded macro-block to the memory unit 3, see col. 11, lines 39 – 50).

Although, Yoshioka '583 teaches decoding macro-blocks and storing, e.g., writing, the decoded macro-blocks to the memory, composed of writing decoded luminance matrix blocks (Y) and decoded chrominance matrix blocks (Cb) and (Cr) to the memory.

Yoshioka '583 is silent in regards to explicit of “five macro-blocks and the arrangement of writing five matrices to the memory; and the first portion, second portion, and the third portion being contiguous”.

Uchida '486 teaches the above-mentioned claimed limitations are well known in the art. In particular, Uchida '486 teaches that, compression operation is applied to

Art Unit: 2621

every five macro-blocks and writing five macro-blocks to the memory areas (i.e., col. 7, lines 26 – 41, col. 15, lines 20 – 21), and further teaches; writing five matrices of luminance pixels to a first portions of the memory (please see, col. 7, lines 26 – 41 of Uchida, indicating five macro- blocks is written in five memory areas, and further figs. 3, 5, 8 and 11 of Uchida, illustrates the order that a_macro-block is written in the memory areas, matrices of luminance pixels Y is written to a first portion of the memory as shown in fig. 11, see col. 7, lines 44 – 57 of Uchida, it is cleared that each one of the five macro-blocks would be written to the memory in the same order as shown in fig. 11 for each macro-block, e.g., five luminance matrices Y would be written to the first five portion of the memory); writing a first five matrices of chrominance pixels to a second five portions of the memory (please see, col. 7, lines 26 – 41 of Uchida, indicating five macro-blocks is written in five memory areas, and further fig. 11 of Uchida, illustrates the order that a macro-block is written in the memory areas, matrices of chrominance R-Y (Cr) is written to the second portion of the memory as shown in fig. 11, see col. 7, lines 26 – 57 of Uchida, it is cleared that each one of the five macro-blocks would be written to the memory in the same order as shown in fig. 11 for each macro-block, e.g., five chrominance matrix R-Y (Cr) would be written to a second five portions of the memory); writing a second five matrices of chrominance to a third portion of the memory (please see, col. 7, lines 26 – 41 of Uchida, indicating five macro- blocks is written in five memory areas, and further fig. 11 of Uchida, illustrates the order that a macro-block is written in the memory areas, matrices of chrominance B-Y (Cb) is written to a third portion of the memory as shown in figs. 3 and 11, see col. 7, lines 44 – 57 of Uchida, it

Art Unit: 2621

is cleared that each one of the five macro-blocks would be written to the memory in the same order as shown in fig. 11 for each macro-block, e.g., five matrices of chrominance B-Y (Cb) would be written to a third portion of the memory); and the first five portions, second five portions, and third five portions being contiguous (i.e., fig. 11 of Uchida, illustrates the order that the luminance matrices Y and Chrominance matrix (Cr) and (Cb) for each macro-block is written to the first, second and third portions of the memory in a continuous/contiguous manner, it is cleared that each one of the five macro-blocks would be written to the memory in the same order and in a continuous/contiguous manner as shown in fig. 11 of Uchida).

In view of the above, having the digital signal processing of Yoshioka showing compression operation is applied to macro-blocks and writing/storing decoded macro-blocks to the memory, and given the well-established teaching of Uchida where the compression operation is applied to every five macro-blocks and writing five macro-blocks to the memory areas, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the digital signal processing of Yoshioka as taught by Uchida, since Uchida suggest in col. 2, lines 57 – 58 that such a modification would improved image quality in the high speed reproduction of the digital video signal.

Regarding claim 5, the limitations claimed are substantially similar to claim 1 above, and is the circuit of the method of claim 1 for string macro-blocks in a memory, therefore the ground for rejecting the method of claim 1 also applies to the circuit claim; and as for the additional limitation, a computer readable medium storing an executable

Art Unit: 2621

instruction (i.e., figs. 3 - 4, it is cleared that the software/instruction is necessitated by the processing units as shown in figs. 3 - 4 in order to carry on the process; such as, decoding macro-blocks, see col. 3, lines 51 – 67 and col. 11, lines 39 - 50), wherein the instruction causes, writing the macro-block to the memory (i.e., as shown in fig. 3, the decoded block/macro-block is written/stored to the memory unit 3, see col. 11, lines 39 – 50).

Regarding claim 7, the limitations claimed are substantially similar to claim 3 above, and is the circuit of the method of claim 3 for string macro-blocks in a memory, therefore the ground for rejecting the method of claim 3 also applies to the circuit claim; and as for the additional limitation, a computer readable medium storing an executable instruction (i.e., figs. 3 - 4, it is cleared that the software/instruction is necessitated by the processing units as shown in figs. 3 - 4 in order to carry on the process; such as, decoding macro-blocks, see col. 3, lines 51 – 67 and col. 11, lines 39 - 50), wherein the instruction causes, writing the macro-block to the memory (i.e., as shown in fig. 3, the decoded block/macro-block is written/stored to the memory unit 3, see col. 11, lines 39 – 50).

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (US 7,079,583) in view of Uchida (US 5,461,486) further in view of Brooks Jr. et al. (US 4,575,814).

Regarding claim 9, the combination of Yoshioka and Uchida is silent in regards to explicit of, data word is part of the second portion and another portion of the single data word is part of the third portion.

Gafken (i.e., figs. 3 and 5, abstract, col. 5, lines 14-25 and 41-55) teaches plurality of memory devices/sections to load portion of data associated with a first address word into a first cell and another portion to another cell of memory, in order to limit the capacity of memory storage to only what is required in a particular system to reduce costs and improve portability.

In view of the above, having the digital signal processing of Yoshioka showing compression operation is applied to macro-blocks and writing/storing decoded macro-blocks to the memory, and given the well-established teaching of Gafken by interfacing a memory sub-system data bus, in order to limit the capacity of memory storage to only what is required in a particular system to reduce costs and improve portability, as suggested by Gafken (i.e., col. 3, lines 60-62).

Response to Arguments

9. Applicant's arguments filed 11/13/2008 have been fully considered but they are not persuasive.

Response to remarks:

Applicant asserts (remarks; page 7, last paragraph) that Uchida does not teach "writing a matrix of decoded luminance pixels to a first portion of the memory and also second and third portion".

However; examiner relied on Yoshioka '583 for writing matrix of decoded luminance pixels and also chrominance pixels in the memory unit 3 (please see, figs. 3 and 5, col. 11, lines 39 – 50 and col. 14, lines 30 - 32 of Yoshioka); and examiner relied

Art Unit: 2621

on the secondary reference, Uchida to show the known arrangement of writing matrices in the memory, as specified in the claim.

and also indicates storing of the compressed video data in the memory 3 (please see, col. 13, lines 16 – 20 and col. 20, lines 55 – 57 of Yoshioka). Yoshioka '583 fails to show the arrangement of writing/storing decoded video data composed of matrix of luminance pixels and matrix of chrominance pixels in the memory, as specifies in the claim. Therefore, it is reasonable to use the memory arrangement as suggested by the secondary reference to modify the memory unit as disclosed by the primary reference, in order to minimize overflowing of the memory area, as suggested by the Uchida (i.e., col. 7, lines 61 – col. 8, lines 3).

Contact

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Behrooz Senfi whose telephone number is 571-272-7339. The examiner can normally be reached on M-F 7:00-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on 571-272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2621

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Behrooz Senfi/
Examiner
Art Unit 2621